AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A data signal line driving method ~~for driving a plurality of data signal lines respectively so as to fetch a multiphased video signal via a plurality of video signal lines into the data signal lines,~~where n, n>1, video signal lines supply a multiphased video signal in parallel to m, m>1, data fetching blocks, each data fetching block including n data line groups and each data line group including n sequential data signal lines and driving contiguous columns of a display, the data signal lines each having an associated sampling switch that connects each data signal line to a video signal line such that n data signals lines are alternately connected to the same video signal line with an interval of another n data signal lines therebetween,

~~data signal line groups, each including a predetermined number of adjacent data signal lines sequentially connected to each video signal line, being regarded as a single block, the number of data signal line groups being equal to the number of the video signal lines in each block,~~

said method comprising:

fetching the video signal from the video signal lines, via n sampling signals, into the data signal lines in each block in response to ~~a~~ timing ~~pulse~~ pulses generated by ~~a predetermined~~ n ~~number of~~ shift registers provided with respect to each block, the ~~predetermined number of~~ n shift registers being connected such that the blocks are driven sequentially~~equal to the number of data signal lines included in each data signal line group~~, there being performed a first driving in which ~~all~~ the n shift registers in ~~the~~ each block are driven sequentially to provide n sequential

output signals and each sampling signal in the block being responsive to a corresponding output signal such that the sampling signals in the block are activated sequentially~~and individual data signal lines of each data signal line group in the block are driven simultaneously so as to fetch the video signal from the video signal lines into the data signal lines~~, and there being performed a second driving in which only one shift register in the block is driven to provide one output signal and all ~~and all data signal lines~~sampling signals in the block are responsive to the one output signal such that all sampling signals in the block are activated simultaneously~~in each data signal ine group in the block are driven simultaneously so as to fetch the video signal from the video signal lines into the data signal lines~~.

2. (Currently amended) A data signal line driving method where n, n>1, video signal lines supply a multiphased video signal having a plurality of color signals in parallel to m, m>1, data fetching blocks, each data fetching block including n data line groups and each data line group including n sequential data signal lines and driving contiguous columns of a display, the data signal lines each having an associated sampling switch that connects each data signal line to a video signal line such that n data signals lines are alternately connected to the same video signal line with an interval of another n data signal lines therebetween~~for driving a plurality of data signal lines respectively so as to (i) multiphase a video signal having a plurality of color signals and (ii) fetch the video signal via a plurality of video signal lines into the data signal lines~~,

each video signal line including a plurality of divisional video signal lines divided so as to respectively correspond to the color signals,

~~data signal line groups, each including a predetermined number of adjacent data signal lines for fetching a single color signal that are sequentially connected to each divisional video signal line, being regarded as a single block, the number of data signal line groups being equal to the number of video signal lines in each block~~,

said method comprising:

fetching the video signal from the video signal lines, via n sampling signals, into the data signal lines in each block in response to timing pulses generated by n shift registers provided with respect to each block, the n shift registers being connected such that the blocks are driven sequentially, there being performed a first driving in which the n shift registers in each block are driven sequentially to provide n sequential output signals and each sampling signal in the block being responsive to a corresponding output signal such that the sampling signals in the block are activated sequentially, and there being performed a second driving in which only one shift register in the block is driven to provide one output signal and all sampling signals in the block are responsive to the one output signal such that all sampling signals in the block are activated simultaneously~~fetching the video signal from the video signal lines into the data signal lines in each block in response to a timing pulse generated by a predetermined number of shift registers provided with respect to each block, the predetermined number of shift registers being equal to the number of data signal lines included in each data signal line group, there being performed a first driving in which all shift registers in the block are driven and individual data signal lines of each data signal ine group in the block are driven simultaneously so as to fetch the video signal from the video signal lines, and there being performed a second driving in which one shift register in the block is driven and all data signal lines in each data signal line group in the block~~

~~are driven simultaneously so as to fetch the video signal from the video signal lines in to the data signal lines~~.

3. (Currently amended) A data signal line driving circuit, which drives a plurality of data signal lines respectively so as to fetch a multiphased video signal via a plurality of video signal lines into the data signal lines, comprising:

n, n>1, video signal lines configured to supply a multiphased video signal having a plurality of color signals in parallel to m, m>1, data fetching blocks, each data fetching block including n data line groups and each data line group including n sequential data signal lines and driving contiguous columns of a display, the data signal lines each having an associated sampling switch that connects each data signal line to a video signal line such that n data signals lines are alternately connected to the same video signal line with an interval of another n data signal lines therebetween~~data signal line groups, each including a predetermined number of adjacent data signal lines sequentially connected to each video signal line, the data signal line groups being regarded as a single block, the number of data signal line groups being equal to the number of video signal lines in each block~~; and

a video signal fetching section for fetching the video signal from the video signal lines into the data signal lines in each block via n sampling signals,

the video signal fetching section including ~~a predetermined number of~~n shift registers provided with respect to each block, the n shift registers being connected such that the blocks are driven sequentially, the n shift registers configured to generate timing pulses ~~for generating a timing pulse~~ with which the video signal is fetched from the video signal lines into the data signal lines~~, the shift registers being provided with respect to each block, the predetermined~~

~~number of shift registers being equal to the number of data signal lines included in each data signal line group~~,

the video signal fetching section performing:

~~first driving in which all shift registers in the block are driven and individual data signal lines of each data signal line group in the block are driven simultaneously so as t fetch the video signal from the video signal lines into the data signal lines~~a first driving in which the n shift registers in each block are driven sequentially to provide n sequential output signals and each sampling signal in the block being responsive to a corresponding output signal such that the sampling signals in the block are activated sequentially; and

a second driving in which only one shift register in the block is driven to provide one output signal and all sampling signals in the block are responsive to the one output signal such that all sampling signals in the block are activated simultaneously~~second driving in which one shift register in the block is driven an all data signal lines in each data signal line group in the block are driven simultaneously so as to fetch the video signal from the video signal lines into the data signal lines~~.

4. (Previously presented) The data signal line driving circuit as set forth in claim 3, wherein the video signal fetching section includes drive switching means for switching between (i) first driving in which the data signal lines of one of the data signal line groups in the block and the data signal lines of another one of the data signal line groups in the block are driven at the same time and (ii) second driving in which all the data signal lines of the data signal line groups are driven at the same time.

5. (Currently amended) The data signal line driving circuit as set forth in claim 4, wherein:

~~the video signal fetching section includes one or more shift registers for generating a timing pulse causing the video signal to be fetched from the video signal lines to the data signal lines, and~~

the drive switching means switches between the first driving and the second driving so that the number of the shift registers that operate is varied in switching between the first driving and the second driving.

6. (Previously Presented) The data signal line driving circuit as set forth in claim 5, wherein the video signal fetching section includes stopping means for stopping operation of the shift register which is not required in driving the data signal lines after switching the drive switching means between the first driving and the second driving.

7. (Previously Presented) The data signal line driving circuit as set forth in claim 3, wherein the video signal fetching section includes a drive switching circuit for switching between (i) first driving in which the data signal lines of one of the data signal line groups in the block and the data signal lines of another one of the data signal line groups in the block are driven at the same time and (ii) second driving in which all the data signal lines of the data signal line groups are driven at the same time.

8. (Currently amended) The data signal line driving circuit as set forth in claim 7, wherein:

~~the video signal fetching section includes one or more shift registers for generating a timing pulse causing the video signal to be fetched from the video signal lines to the data signal lines, and~~

the drive switching circuit switches between the first driving and the second driving so that the number of the shift registers that operate is varied in switching between the first driving and the second driving.

9. (Previously Presented) The data signal line driving circuit as set forth in claim 8, wherein the video signal fetching section includes stopping means for stopping operation of the shift register which is not required in driving the data signal lines after switching the drive switching circuit between the first driving and the second driving.

10. (Original) The data signal line driving circuit as set forth in claim 3, wherein the data signal line groups are data signal line sets each of which is made up of a predetermined number of data signal lines respectively corresponding to color signals contained in the video signal fetched into the data signal lines.

11. (Currently amended) A data signal line driving circuit, which drives a plurality of data signal lines respectively so as to (i) multiphase a video signal having a plurality of color signals and (ii) fetch the video signal into the data signal lines,

each video signal line including a plurality of divisional video signal lines divided so as to respectively correspond to the color signals, said circuit comprising:

~~data signal line groups, each including a predetermined number of adjacent data signal lines for fetching a single color signal that are sequentially connected to each divisional video signal line, the data signal line groups being regarded as a single block, the number of data signal line groups being equal to the number of video signal lines in each block~~n, n>1, video signal lines configured to supply a multiphased video signal having a plurality of color signals in parallel to m, m>1, data fetching blocks, each data fetching block including n data line groups and each data line group including n sequential data signal lines for fetching a single color signal and driving contiguous columns of a display, the data signal lines each having an associated sampling switch that connects each data signal line to a video signal line such that n data signals lines are alternately connected to the same video signal line with an interval of another n data signal lines therebetween; and

a video signal fetching section for fetching the video signal from the video signal lines into the data signal lines in each block~~.~~ via n sampling signals,

the video signal fetching section including ~~a predetermined number of~~n shift registers provided with respect to each block, the n shift registers being connected such that the blocks are driven sequentially, the n shift registers configured to generate timing pulses ~~for generating a timing pulse~~ with which the video signal is fetched from the video signal lines into the data signal lines~~, the shift registers being provided with respect to each block, the predetermined number of shift registers being equal to the number of data signal lines included in each data signal line group~~,

the video signal fetching section performing

a first driving in which the n shift registers in each block are driven sequentially to provide n sequential output signals and each sampling signal in the block being responsive to a

corresponding output signal such that the sampling signals in the block are activated sequentially~~first driving in which all shift registers in the block are driven and individual data signal lines of each data signal line group in the block are driven simultaneously so as to fetch the video signal from the video signal lines into the data signal lines~~, and

a second driving in which only one shift register in the block is driven to provide one output signal and all sampling signals in the block are responsive to the one output signal such that all sampling signals in the block are activated simultaneously~~second driving in which one shift register in the block is driven and all data signal lines in each data signal line group in the block are driven simultaneously so as to fetch the video signal form the video signal lines into the data signal lines~~.

12. (Previously Presented) The data signal line driving circuit as set forth in claim 11, wherein the video signal fetching section includes drive switching means for switching between (i) first driving in which the data signal lines of one of the data signal line groups in the block and the data signal lines of another one of the data signal line groups in the block are driven at the same time and (ii) second driving in which all the data signal lines of the data signal line groups are driven at the same time.

13. (Currently amended) The data signal line driving circuit as set forth in claim 12, wherein:

~~the video signal fetching section includes one or more shift registers for generating a timing pulse causing the video signal to be fetched from the video signal lines to the data signal lines, and~~

the drive switching means switches between the first driving and the second driving so that the number of the shift registers that operate is varied in switching between the first driving and the second driving.

14. (Previously Presented) The data signal line driving circuit as set forth in claim 13, wherein the video signal fetching section includes stopping means for stopping operation of the shift register which is not required in driving the data signal lines after switching the drive switching means between the first driving and the second driving.

15. (Previously Presented) The data signal line driving circuit as set forth in claim 11, wherein the video signal fetching section includes a drive switching circuit for switching between (i) first driving in which the data signal lines of one of the data signal line groups in the block and the data signal lines of another one of the data signal line groups in the block are driven at the same time and (ii) second driving in which all the data signal lines of the data signal line groups are driven at the same time.

16. (Currently amended) The data signal line driving circuit as set forth in claim 15, wherein:

~~the video signal fetching section includes a shift register for generating a timing pulse causing the video signal to be fetched from the video signal lines to the data signal lines, and~~

the drive switching circuit switches between the first driving and the second driving so that the number of the shift registers that operate is varied in switching between the first driving and the second driving.

17. (Previously Presented) The data signal line driving circuit as set forth in claim 16, wherein the video signal fetching section includes stopping means for stopping operation of the shift register which is not required in driving the data signal lines after switching the drive switching circuit between the first driving and the second driving.

Claim 18. (Currently amended) The data signal line driving circuit as set forth in claim 11, wherein the data signal line groups are ~~data signal line~~ made up of sets of data signal lines, ~~each of which is made up of a predetermined number of the data signal lines corresponding to color signals contained in the video signal fetched into the data signal lines, and wherein the number of divisional video signal lines is the same as the number of data signal lines connected to each of the divisional video signal lines~~ the number of the sets being equal to the number of colors corresponding to video signals each fetched into the data signal lines.

19. (Currently amended) A display device, comprising:

a display panel which includes (i) a plurality of data signal lines, (ii) a plurality of scanning signal lines provided so as to cross the data signal lines, and (iii) pixels provided on intersections of the data signal lines and the scanning signal lines, a video signal for displaying an image being fetched from the data signal lines into the pixels in synchronism with a scanning signal supplied from the scanning signal lines, said video signal being retained;

a data signal line driving circuit for outputting the video signal to the data signal lines in synchronism with a predetermined timing signal; and

a scanning signal line driving circuit for outputting the scanning signal to the scanning signal lines in synchronism with a predetermined timing signal, said video signal being multiphased, and being supplied to the data signal lines via a plurality of video signal lines, each video signal line including a plurality of divisional video signal lines divided so as to respectively correspond to color signals wherein

the data signal line driving circuit, which drives said plurality of data signal lines respectively so as to fetch the multiphased video signal via said plurality of video signal lines into the data signal lines, includes:

~~data signal line groups, each including a predetermined number of adjacent data signal lines for fetching a single color signal that are sequentially connected to each divisional video signal line, the data signal line groups being regarded as a single block, the number of data signal line groups being equal to the number of video signal lines in each block~~where n, n>1, video signal lines supply a multiphased video signal in parallel to m, m>1, data fetching blocks, each data fetching block including n data line groups and each data line group including n sequential data signal lines and driving contiguous columns of a display, the data signal lines each having an associated sampling switch that connects each data signal line to a video signal line such that n data signals lines are alternately connected to the same video signal line with an interval of another n data signal lines therebetween; and

a video signal fetching section for fetching the video signal from the video signal lines into the data signal lines in each block via n sampling signals,

the video signal fetching section including n shift registers provided with respect to each block, the n shift registers being connected such that the blocks are driven sequentially, the n shift registers configured to generate timing pulses with which the video signal is fetched from the video signal lines into the data signal lines~~the video signal fetching section including a predetermined number of shift registers for generating a timing pulse with which the video signal is fetched from the video signal lines into the data signal lines, the shift registers being provided with respect to each block, the predetermined number of shift registers being equal to the number of data signal lines included in each data signal line group~~,

the video signal fetching section performing

a first driving in which the n shift registers in each block are driven sequentially to provide n sequential output signals and each sampling signal in the block being responsive to a corresponding output signal such that the sampling signals in the block are activated sequentially; and

a second driving in which only one shift register in the block is driven to provide one output signal and all sampling signals in the block are responsive to the one output signal such that all sampling signals in the block are activated simultaneously~~first driving in which all shift registers in the block are driven and individual data signal lines of each data signal line group in the block are driven simultaneously so as to fetch the video signal from the video signal lines into the data signal lines, and~~

~~second driving in which one shift register in the block is driven and all data signal lines in each data signal line group in the block are driven simultaneously so as to fetch the video signal form the video signal lines into the data signal lines~~.

20. (Original) The display device as set forth in claim 19, wherein the data signal line driving circuit, the scanning signal line driving circuit, and the pixels are formed on the same substrate.

21. (Currently amended) A display device, comprising:

a display panel which includes (i) a plurality of data signal lines, (ii) a plurality of scanning signal lines provided so as to cross the data signal lines, and (iii) pixels provided on intersections of the data signal lines and the scanning signal lines, a video signal for displaying an image being fetched from the data signal lines into the pixels in synchronism with a scanning signal supplied from the scanning signal lines, said video signal being retained;

a data signal line driving circuit for outputting the video signal to the data signal lines in synchronism with a predetermined timing signal; and

a scanning signal line driving circuit for outputting the scanning signal to the scanning signal lines in synchronism with a predetermined timing signal, said video signal being multiphased, and being supplied to the data signal lines via a plurality of video signal lines, wherein

the data signal line driving circuit, which drives a plurality of data signal lines respectively so as to (a) multiphase the video signal having a plurality of color signals and (b) fetch the video signal into the data signal lines, each video signal line including a plurality of video signal lines divided so as to respectively correspond to color signals, comprising

~~data signal line groups, each including a predetermined number of adjacent data signal lines for fetching a single color signal that are sequentially connected to each divisional video signal line, the data signal line groups being regarded as a single block, the number of data signal~~

~~line groups being equal to the number of video signal lines in each block~~n, n>1, video signal lines configured to supply a multiphased video signal having a plurality of color signals in parallel to m, m>1, data fetching blocks, each data fetching block including n data line groups and each data line group including n sequential data signal lines for fetching a single color signal and driving contiguous columns of a display, the data signal lines each having an associated sampling switch that connects each data signal line to a video signal line such that n data signals lines are alternately connected to the same video signal line with an interval of another n data signal lines therebetween; and

a video signal fetching section for fetching the video signal from the video signal lines into the data signal lines in each block via n sampling signals,

the video signal fetching section including n shift registers provided with respect to each block, the n shift registers being connected such that the blocks are driven sequentially, the n shift registers configured to generate timing pulses with which the video signal is fetched from the video signal lines into the data signal lines~~the video signal fetching section including a predetermined number of shift registers for generating a timing pulse with which the video signal is fetched from the video signal lines into the data signal lines, the shift registers being provided with respect to each block, the predetermined number of shift registers being equal to the number of data signal lines included in each data signal line group~~,

the video signal fetching section performing

a first driving in which the n shift registers in each block are driven sequentially to provide n sequential output signals and each sampling signal in the block being responsive to a corresponding output signal such that the sampling signals in the block are activated sequentially; and

a second driving in which only one shift register in the block is driven to provide one output signal and all sampling signals in the block are responsive to the one output signal such that all sampling signals in the block are activated simultaneously~~first driving in which all shift registers in the block are driven and individual data signal lines of each data signal line group in the block are driven simultaneously so as to fetch the video signal from the video signal lines into the data signal lines, and~~

~~second driving in which one shift register in the block is driven and all data signal lines in each data signal line group in the block are driven simultaneously so as to fetch the video signal form the video signal lines into the data signal lines~~.

22. (Original) The display device as set forth in claim 21, wherein the data signal line driving circuit, the scanning signal line driving circuit, and the pixels are formed on the same substrate.